

Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently amended) A method of processing an interrupt verification support mechanism in a computer system comprising a processor and an input for external interrupts communicatively coupled to the processor, the method comprising the steps:

(a) processing at least one actual instruction in the processor; and
(b) if an external interrupt request or an interrupt pseudo-instruction is received by the processor, replacing the actual instruction ~~is replaced~~ in an instruction fetch stage of the processor with the pseudo-instruction.

2. (Original) The method of claim 1 comprising :
processing at least one actual instruction in the processor in an instruction pipeline wherein instructions are processed concurrently by an instruction fetch stage, an instruction decode stage, an instruction issue stage, an instruction execute stage and a result write-back stage.

3. (Cancelled).

4. (Original) The method of claim 1 further comprising:
creating the pseudo-instruction by a co-processor connected to the processor.

5. (Original) The method of claim 1 comprising:
simultaneously processing a number of instructions in the processor in an
instruction pipeline with several instruction stages each instruction being in a different
instruction stage at a time.

6. (Currently amended) The method of claim 1 further comprising:
storing at least [[the]] information of [[the]] a program counter of the instruction
which is to be interrupted and [[the]] a sort of interrupt to use in a set of one or more
interrupt registers of the processor.

7. (Currently amended) The method of claim 1 further comprising:
comparing [[the]] data content of a program counter with [[the]] data content of
an interrupt register and replacing the actual instruction with a pseudo-instruction when
the data content of the program counter matches the data content of the interrupt register,
or when an external interrupt is present.

8. (Currently amended) An Interrupt interrupt verification support mechanism
device for a computer system comprising a processor and an input for external interrupt
requests or interrupt pseudo-instructions communicatively coupled to the processor,
wherein the device includes a set of one or more interrupt registers each of which
contains information, the information including at least [[the]] a program counter of the
instruction which is to be interrupted and [[the]] a sort of interrupt to use, so as to enable
the device to process at least one actual instruction, and if an external interrupt request is

received by the processor, the at least one actual instruction is replaced with the pseudo-instruction.

9. (Currently amended) The device of claim 8 wherein
the device further comprises an instruction fetch with a program counter and an interrupt register, the instruction fetch being coupled to a first input of a ~~de-multiplexer~~ multiplexer for transmitting instructions to said ~~de-multiplexer~~ multiplexer, [[the]] a second input of the ~~de-multiplexer~~ multiplexer connected to an interrupt pseudo-instruction input and the program counter connected with the interrupt register by a comparator.

10. (Original) The device of claim 9 wherein
the second input of the ~~de-multiplexer~~ multiplexer is capable of receiving interrupt pseudo-instruction signals or external interrupt requests.

11. (Currently amended) The device of claim 9 wherein
the comparator creates a high level signal only if [[the]] data content of the program counter matches [[the]] data content of the interrupt register.

12. (Currently amended) The device of claim 9 wherein
[[the]] an output of the comparator is connected to [[the]] a first input of an or-operator, and [[the]] a second input of the or-operator is connected to an interrupt controller so as to enable the or-operator to create a high level signal if [[the]] a signal

received from the interrupt controller differs from [[the]] a signal received from the comparator.

13. (Currently amended) The device of claim 9 wherein,
when [[the]] data content of the program counter matches [[the]] data content of the interrupt register, the actual instruction is replaced with a pseudo-instruction.

14. (Original) The device of claim 9 wherein
when an external interrupt request is present at the ~~de-multiplexer~~ multiplexer,
the actual instruction is replaced with an interrupt pseudo-instruction.

15. (Currently amended) The device of claim 9 wherein
[[the]] an instruction coming from [[the]] an output of the ~~de-multiplexer~~
multiplexer is sequentially processed in [[the]] an instruction pipeline of the processor.

16. (Currently amended) The device of claim 9 wherein
[[the]] an instruction pipeline of the processor includes an instruction fetch stage,
an instruction decode stage, an instruction issue stage, an instruction execute stage and a result write-back stage.

17. (Currently amended) The device of claim 9 wherein
the interrupt pseudo-instruction effects [[the]] instruction state stages required by the interrupt pseudo-instruction.

18. (Currently amended) The device of claim 16 wherein
if an interrupt request or an interrupt pseudo-instruction is received by the
processor, the processor is adapted to cancel an instruction that is in the instruction fetch
stage when the interrupt request or the interrupt pseudo-instruction is received and to
reissue the cancelled instruction starting at the instruction fetch stage.

19. (Currently amended) The device of claim 16 wherein
if an interrupt request or an interrupt pseudo-instruction is received by the
processor, the processor is adapted to cancel an instruction that is in any instruction stage
when the interrupt request or the interrupt pseudo-instruction is received and to reissue
the instruction starting at the instruction fetch stage.

20. (Original) The device of claim 8 wherein
the pseudo-instruction is created by a co-processor connected to the processor.

21. (Currently amended) The device of claim [[8]] 20 wherein
the device is a media decoding system, the processor is a core decoder processor
and the co-processor is a decoding accelerator adapted to assist the core processor with a
decoding function.

22. (Original) The device of claim 20 wherein
the processor is a reduced instruction set computer (RISC) processor.

23. (Original) A computer comprising the device of claim 8.

24. (Original) A computer utilizing the method of claim 1.